

Fig. 1 (prior art)

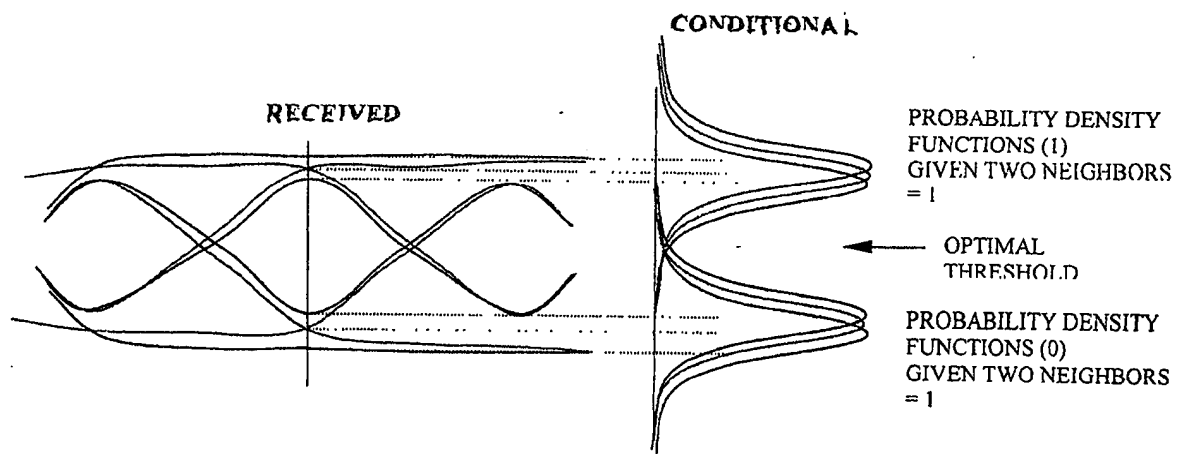


Fig. 2 (prior art)

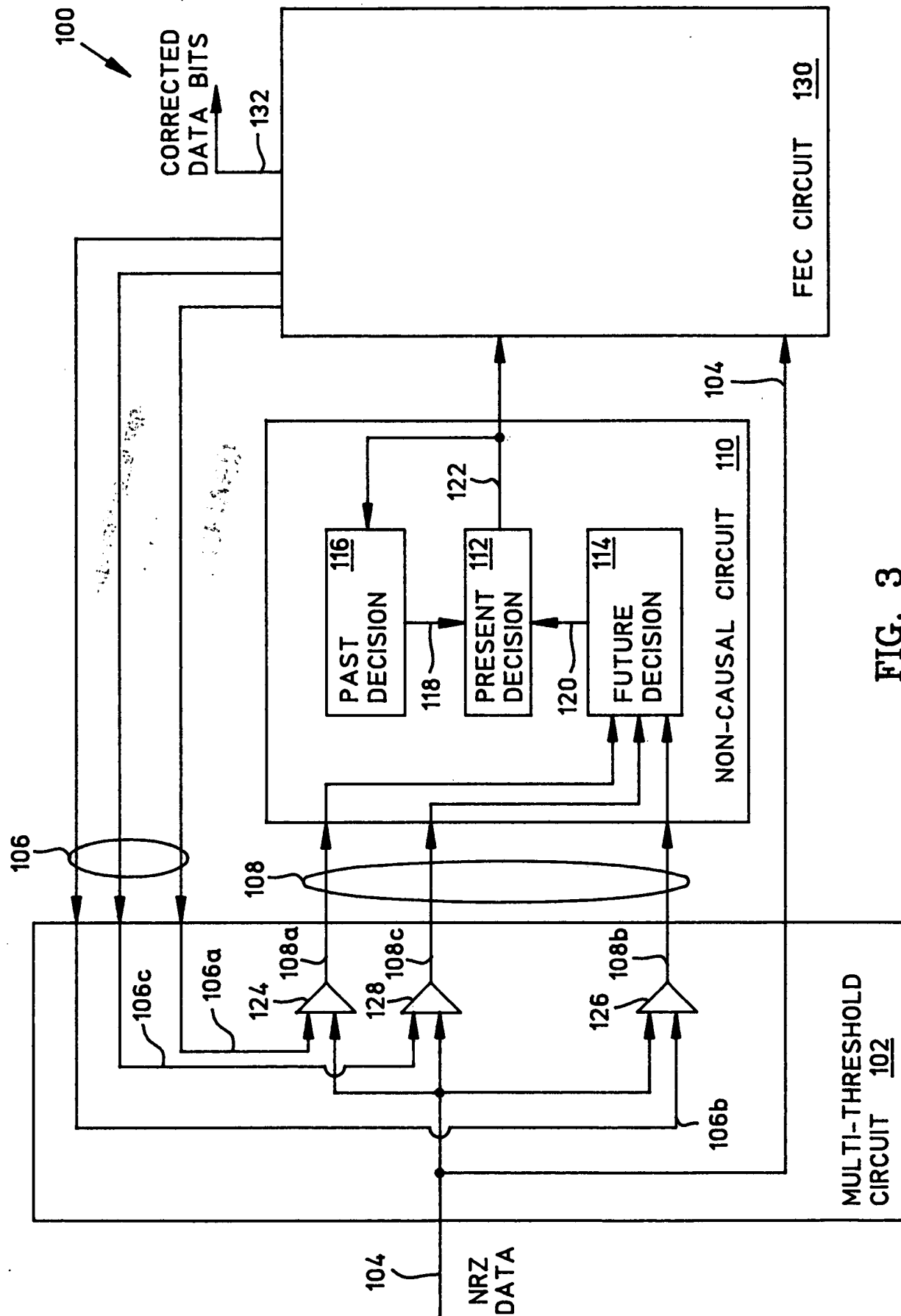


FIG. 3

NRZ data stream inputs

NRZ data stream inputs

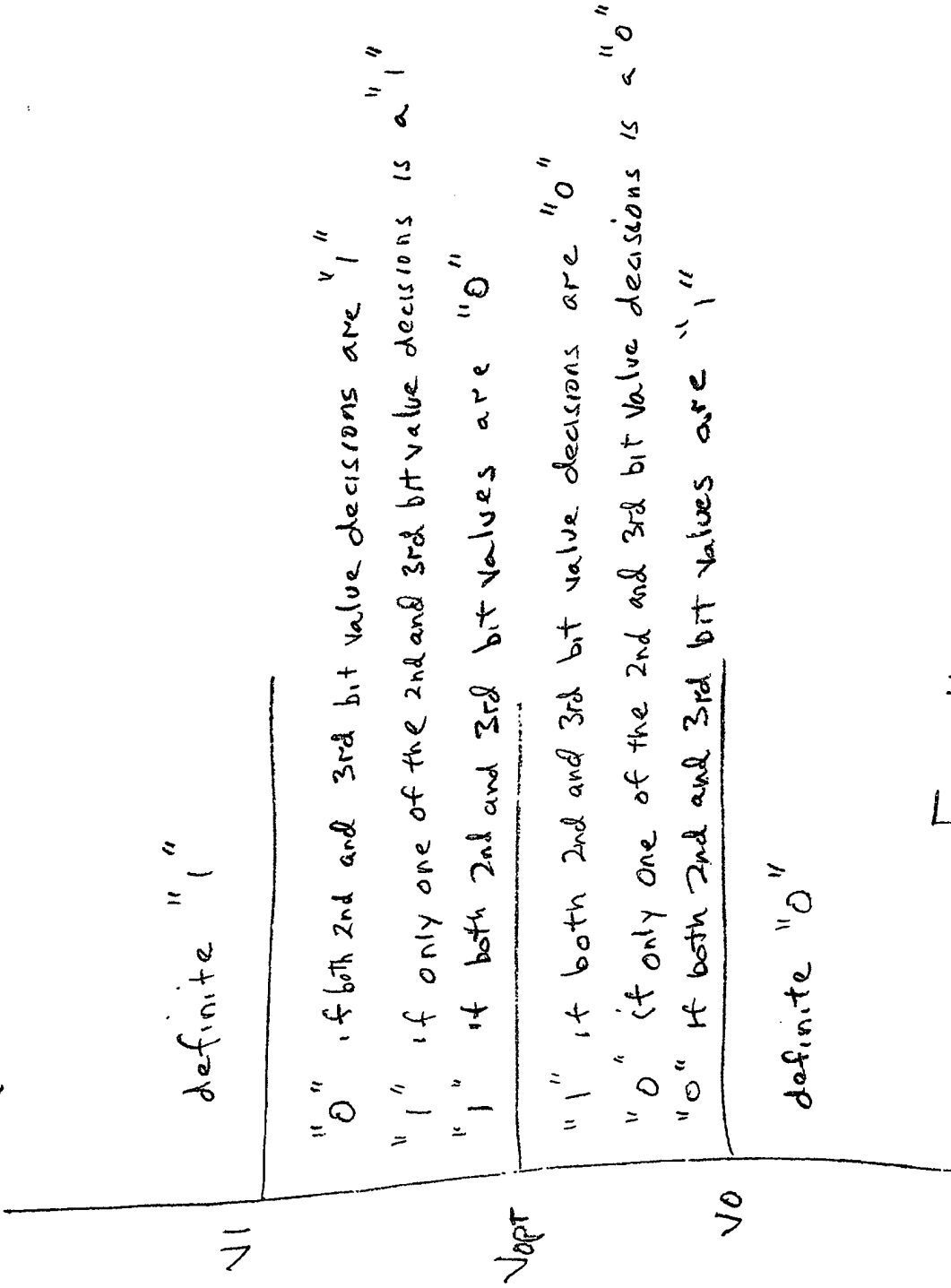


Fig. 4

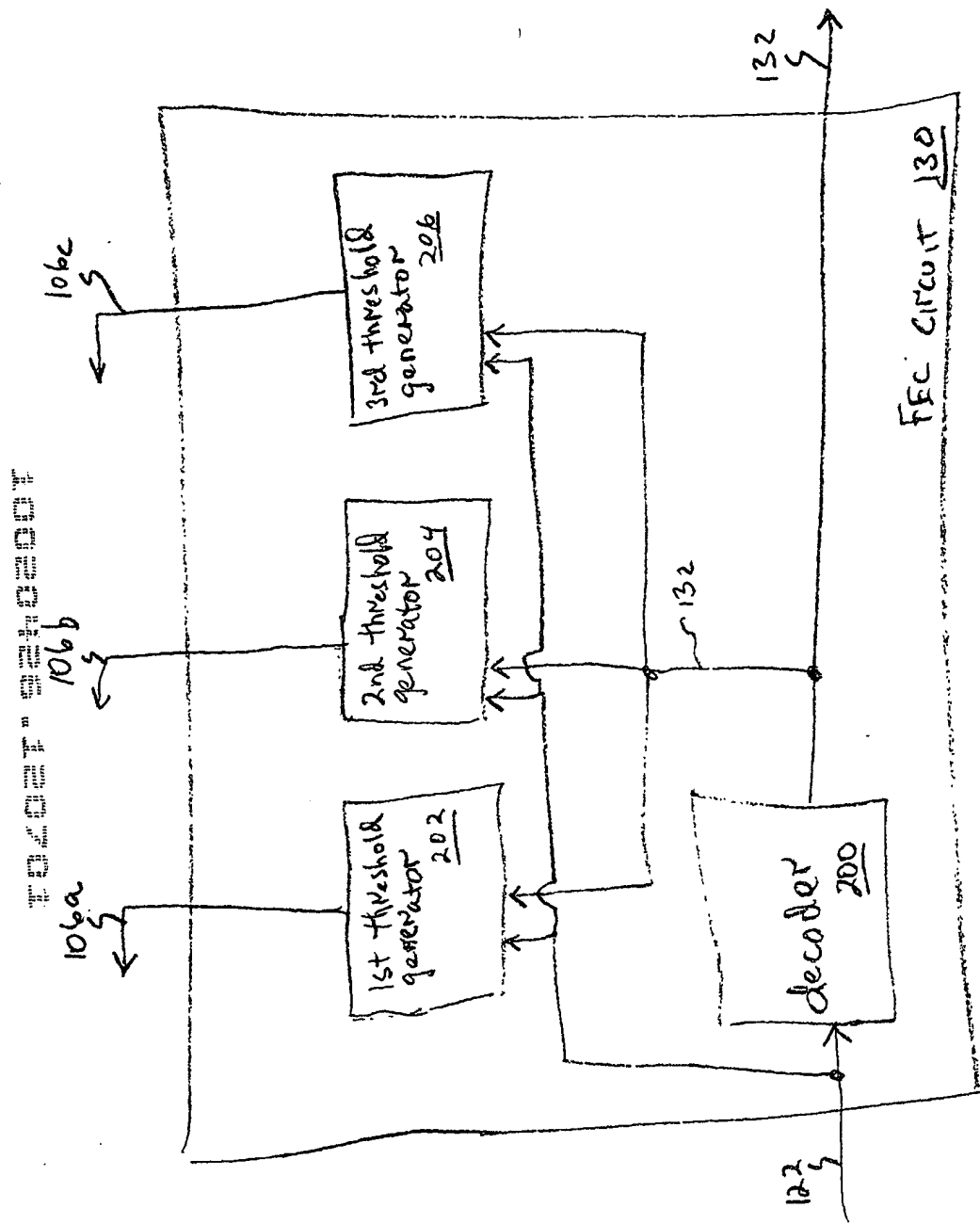
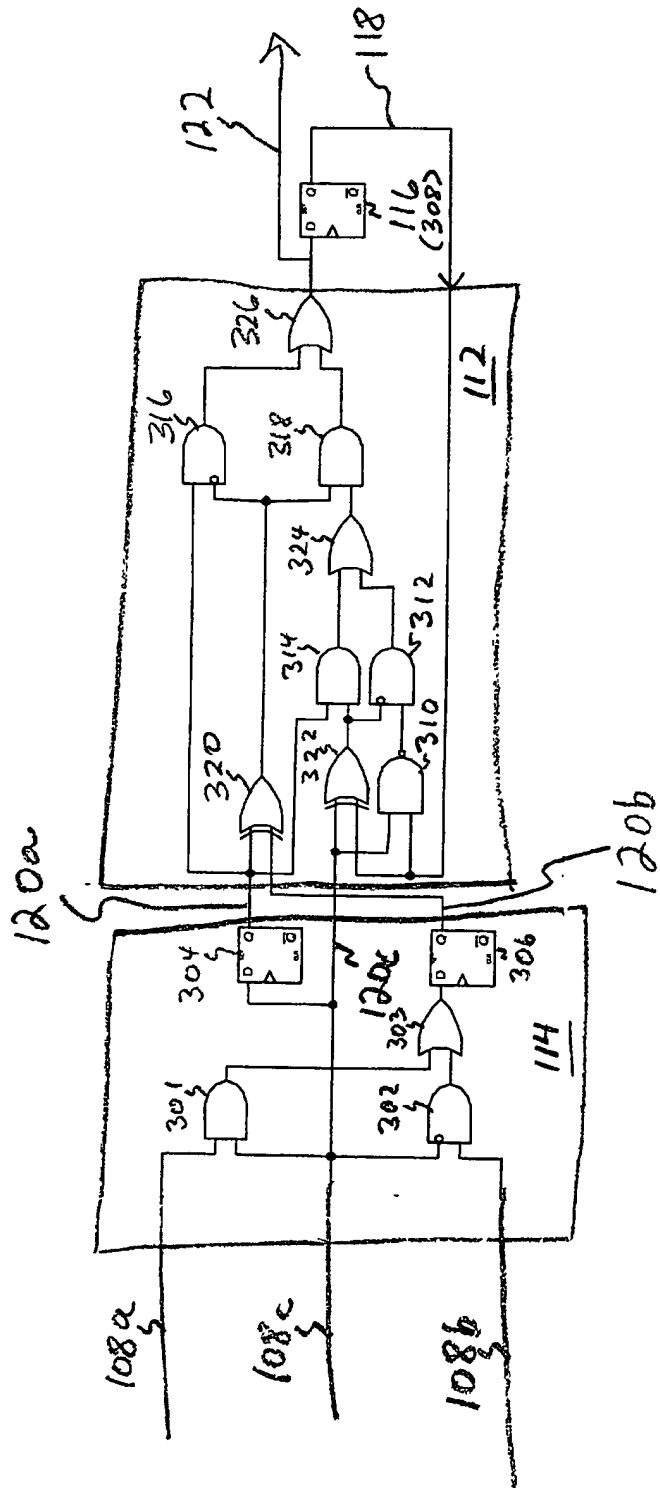


Fig. 5

110

Fig. 7a



FIRST BIT Estimate		2nd bit Value	3rd bit Value	1st bit Value
line 120a	120b			
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Fig. 7b

FIG. 8

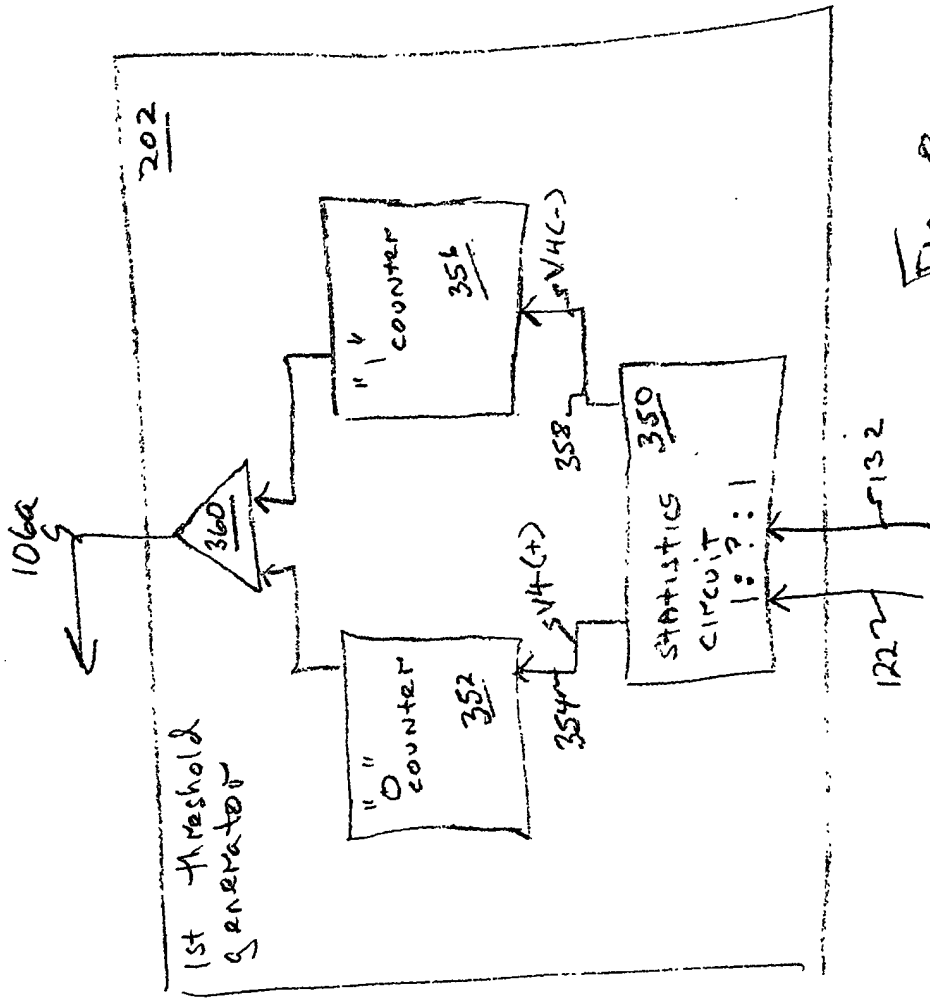


FIG. 8

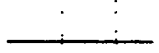

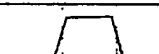
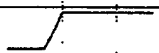

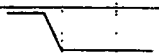
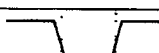
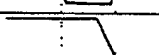

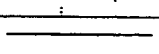
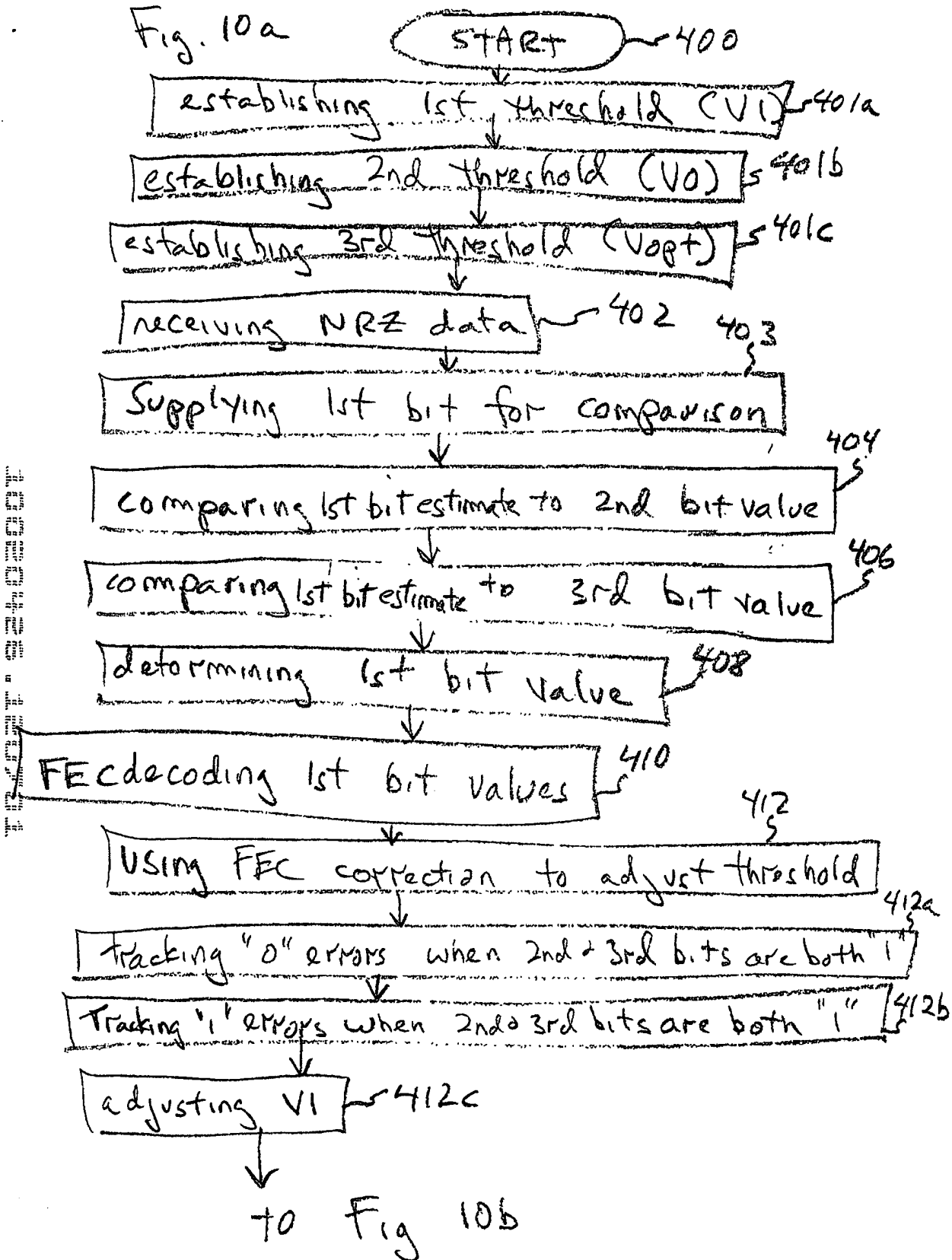
Only One Correction per 3 bit sequence					
Error in the center bit					
Corrected Sequence	Graphic	Affected Counter		Action on Feedback	
		0 cntr	1 cntr	-	+
0 0 0		Cond 1 0 inc		V1 toggle	
0 0 1		Cond 2 0 inc		V2 toggle	
0 1 0			Cond 1 1 inc		V1 Toggle
0 1 1					V2 Toggle
1 0 0		Cond 3 0 inc		V3 Toggle	
1 0 1		Cond 4 0 inc		V4 Toggle	
1 1 0					V3 Toggle
1 1 1			Cond 4 1 inc		V4 Toggle

Fig. 9

Fig. 10a



↓ from Fig 10a
Tracking "0" corrections when 2nd & 3rd bits are both "0" 412d

↓ 412e
Tracking "1" corrections when 2nd & 3rd bits are both "0"

↓
adjusting V_0 412f

↓ 412g
Tracking "0" corrections when only one of the 2nd and 3rd bits is a "1"

↓ 412h
Tracking "1" corrections when only one of the 2nd and 3rd bits is a "1"

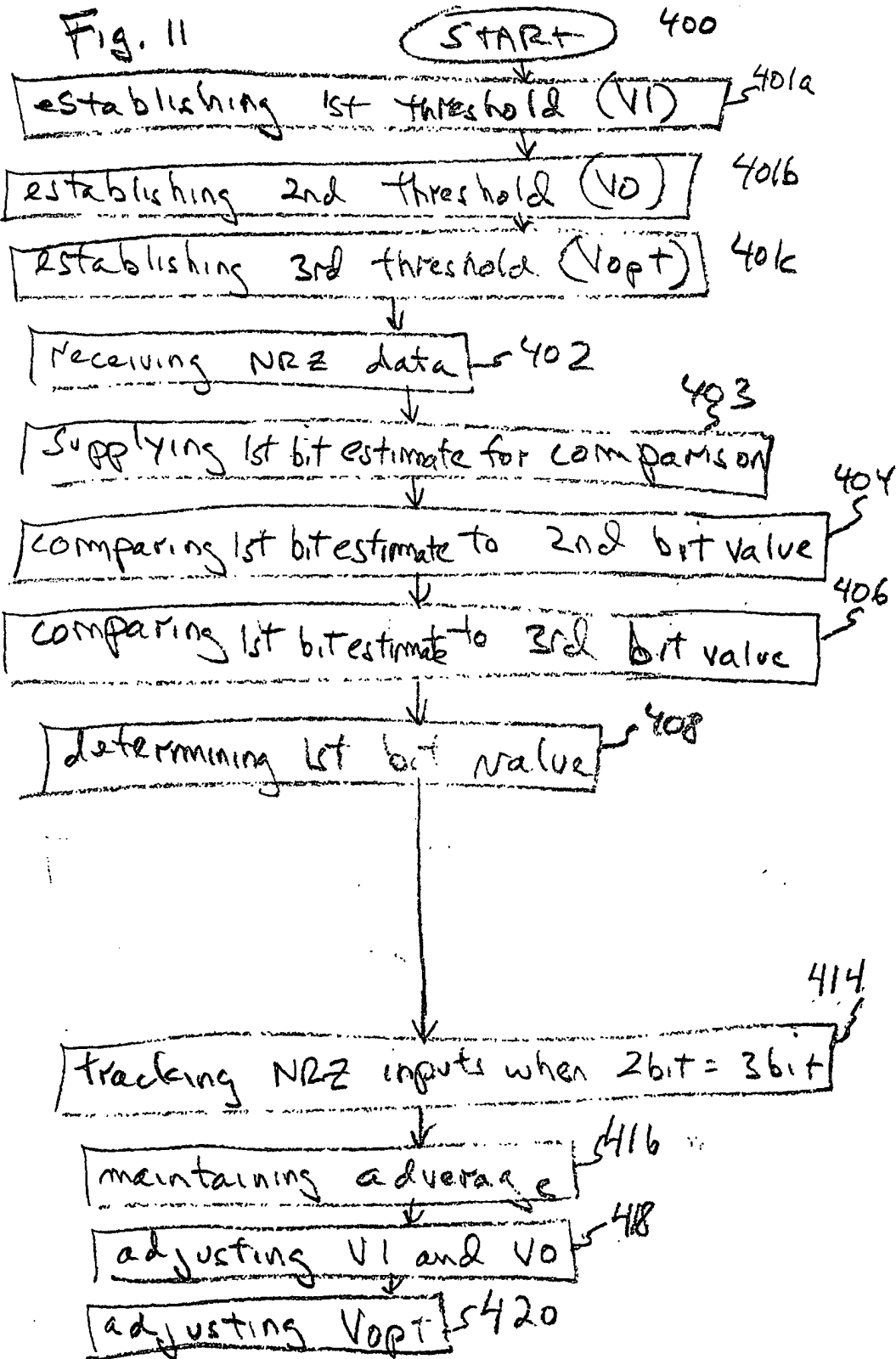
↓
adjusting V_{opt} 412i

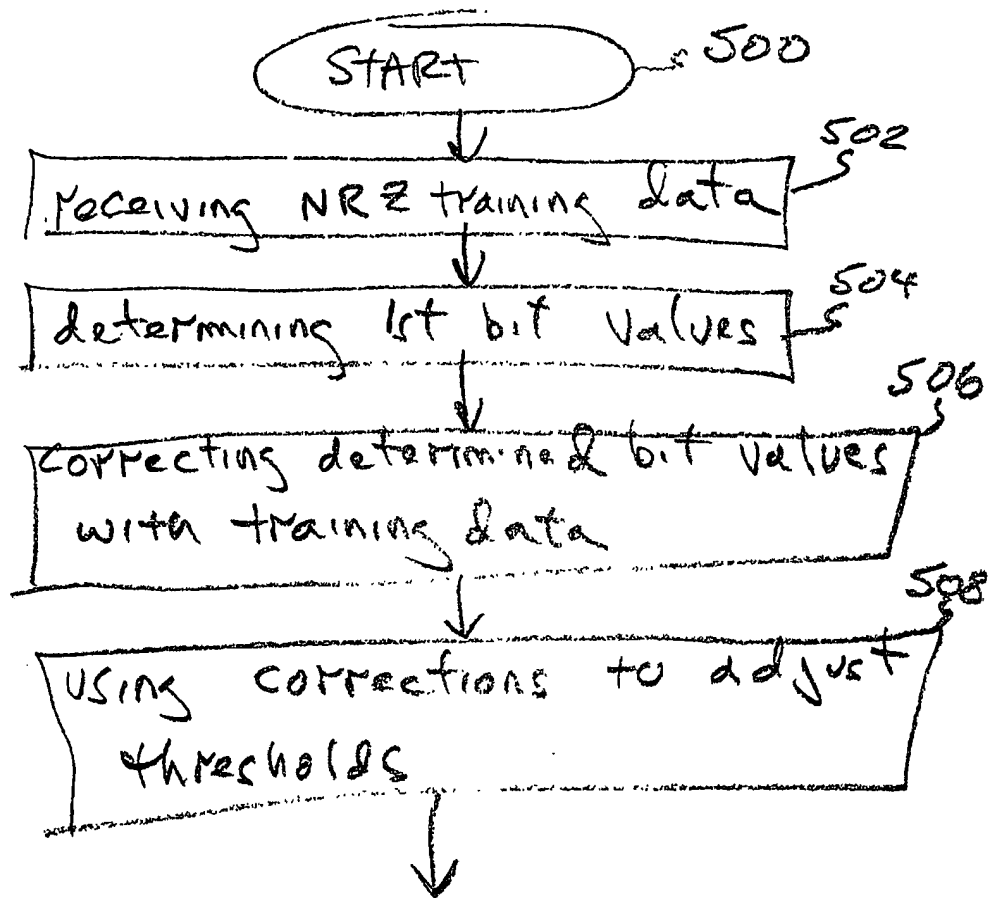
↓ 412j
Tracking corrections when 1st bit value is "1"

↓
adjusting V_{opt} 412k

Fig. 10b

Fig. 11





to step 4012 of
Fig. 10a or Fig. 11

Fig. 12